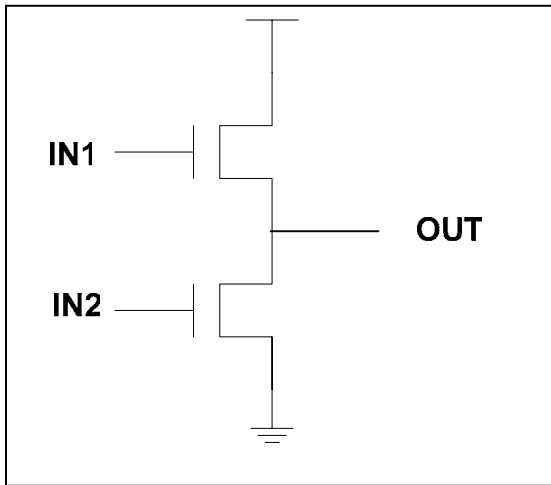


COEN 6501: Digital Design and Synthesis

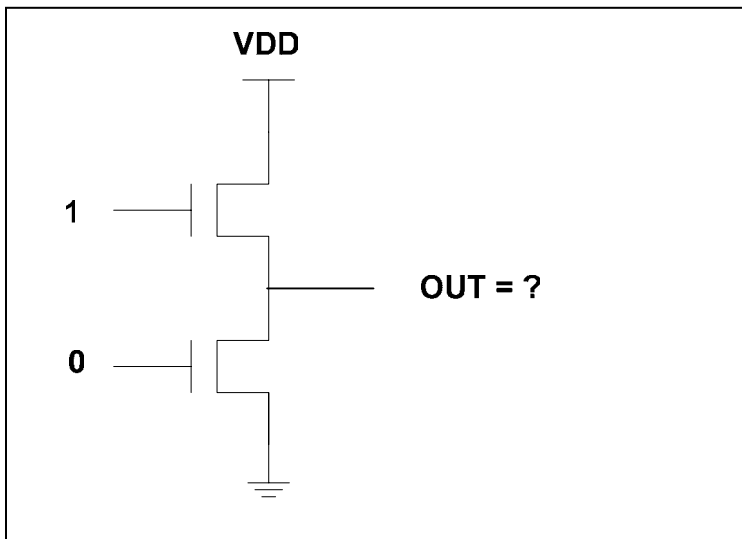
**Lecture Notes supplement to explain why we use the 9 value logic system of
ieee.std_logic_1164**

Take an example of 2 CMOS transistors connected below.

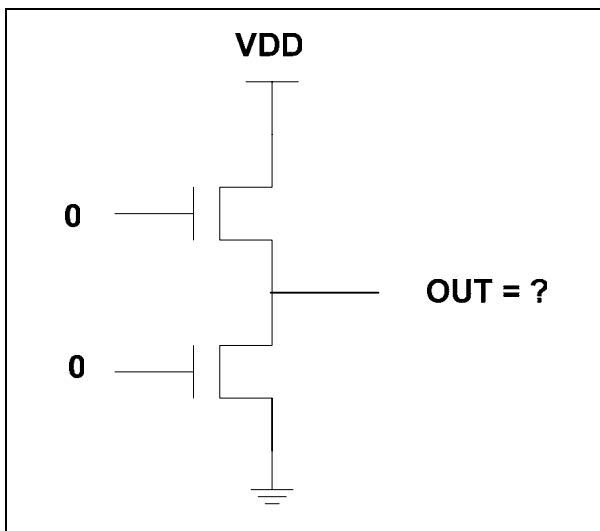
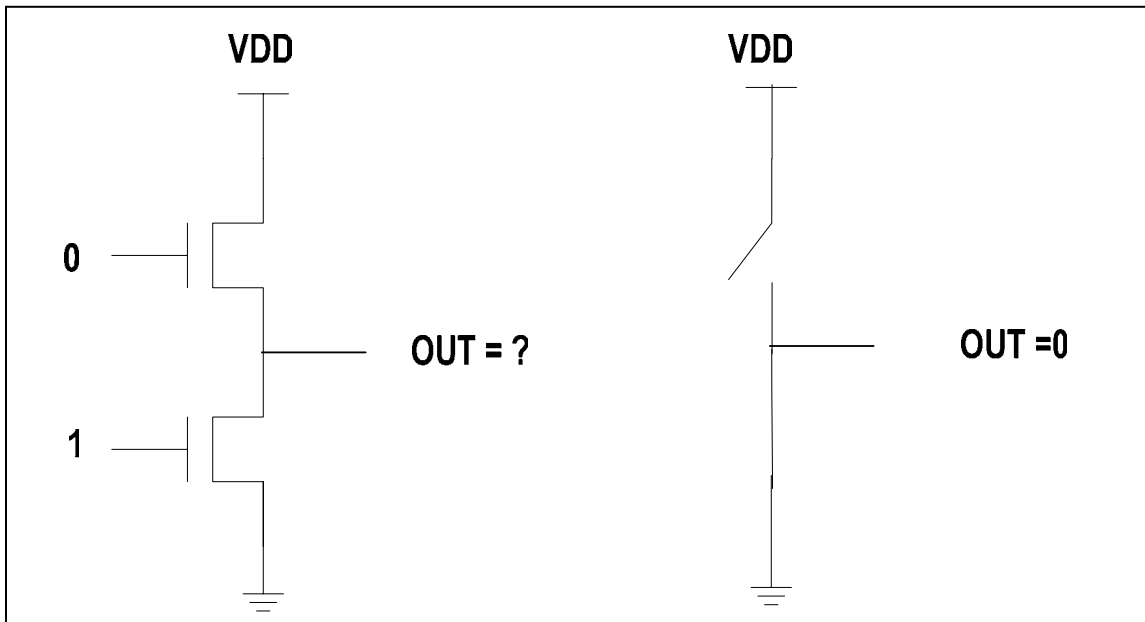
For different input combinations we have different output levels.



If IN1 = 1 , IN2 = 0 , OUTPUT = VDD



If $IN1 = 0$, $IN2 = 1$, $OUTPUT = 0$



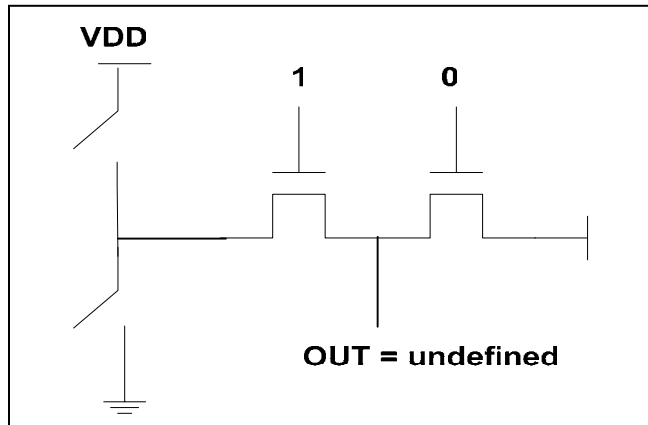
**But what if $IN1 = '0'$, $IN2 = '0'$,
then**

**OUTPUT is in high impedance or just
floating.**

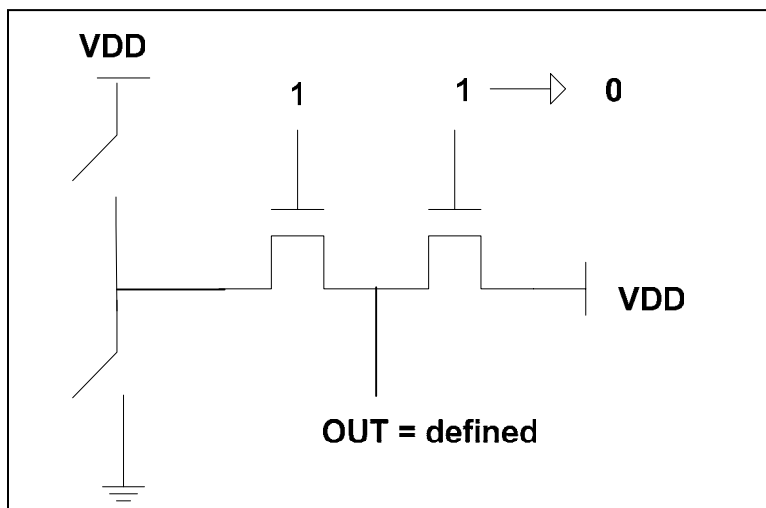
**This is because there is no connection to the
“0” source impedance.**

Hence a need for the Z state.

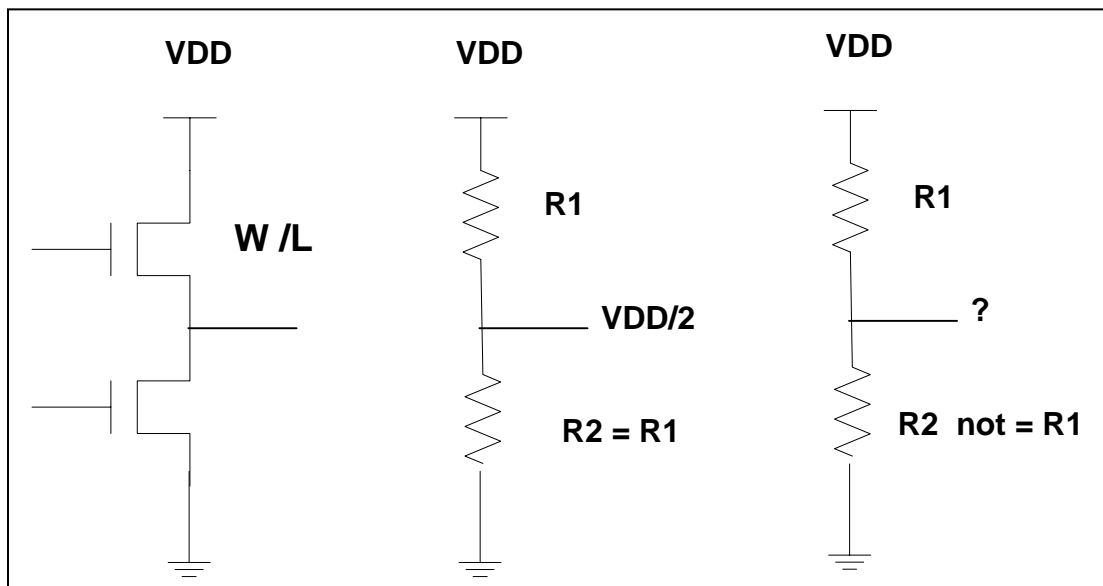
In the other hand how do we represent the storage nodes ?
Look at the Figure below:



If $IN1 = '0'$, $IN2 = '0'$, $IN3 = '1'$, $IN4 = '1' \Rightarrow '0'$
OUTPUT will be high floating first, then the output will take a value depending on the time that the output stays unconnected. During this period the voltage value will decrease. Will it be a '1' or '0'? That depends on the V_h definition.



What if the ratio W/L of various transistors are different ?
 Suppose $R1$ and $R2$ are resistances of transistor 1 and 2,
 if $R1 = R2$ then the output is $V_{dd}/2$ but if $R1 \neq R2$ what will be the output ?
 Then the output will be $V_{dd} * [R2 / (R1 + R2)]$. Is that a '1' or '0' ?



Conclusion

Logic '1' and '0' are not sufficient for defining logic levels.
 For this purpose we use
 use ieee.std_logic_1164.ALL
 In this way we can have other logic levels described by this standard.

```
library ieee;
use ieee.std-logic-1164
This has 9 value system: U,X,0,1,Z,W,L,H,-.
Or
The 46 value system defined as the t-wlogic.
Example:
library std
use std.std-logic.all

port (D,CLK: in t-wlogic; Q:out t-wlogic);
```

OBJECTS:

There are 3 different class objects in VHDL:

- **Constant**

Constant does not change value.

Constant PAI: real := 3.14;

- **Variable**

Changes value immediately. Has no past and no future.

Example. What are the values of A & B defined as variables within a process?

A:=1;

B:=A;

Since these assignments are made immediately then A=1 and B=1.

- **Signal**

Have past, present and future.

Example: What are the values of A & B defined in a concurrent body.

A<='1';

B<=A;

Since there is always some delay associated with signals then in the first assignment A will take a value of 1 after a finite amount of time and B will take the initial value of A whatever it was.

Signal propagation

In the Figure below if $In_1 = y$ then $In_2 = y$ is not a true statement.
This is because of the size and length of the two buses to C2 and C3 are different.

We have to consider time

$In_1 \leq y$ after t_1 ;

$In_2 \leq y$ after t_2 ;

Where $t_1 \gg t_2$

Conclusion there is very much difference between signal and variable.

